STATUTORY INSTRUMENTS

2024 No. 346

The Export Control (Amendment) Regulations 2024

Amendments to the Export Control Order 2008

2.—(1) The Export Control Order 2008(**1**) is amended as follows.

(2) In Schedule 2 (Military Goods, Software and Technology)—

(a) in the Technical Note to entry ML4.b., for "*purpose of ML4.b.*" substitute "*purposes of ML4.b.,*";

(b) in the Note to entry ML7—

(i) for "*Abstract*" substitute "*Abstracts*";

(ii) for "*(e.g. hydrates)*" substitute "*(e.g. hydrates, isotopically-labelled forms or all possible stereoisomers)*";

(c) in the Note to entry ML8—

(i) for "*Abstract*" substitute "*Abstracts*";

(ii) for "*(e.g. hydrates)*" substitute "*(e.g. hydrates, isotopically-labelled forms or all possible stereoisomers)*";

(d) in paragraph 1 of the Technical Note to entry ML8, for "*A 'mixture'*" substitute "*For the purposes of ML8, excluding ML8.c.11. and ML8.c.12., a 'mixture'*";

(e) in paragraph 2 of the Technical Note to entry ML8, for "*Particle size is*" substitute "*For the purposes of ML8, particle size is*";

(f) in the Technical Note in entry ML8.a., for "*An 'explosive co-crystal'*" substitute "*For the purposes of ML8.a., an 'explosive co-crystal'*";

(g) in entry ML8.d.3., after Note 2 on a new line insert—

"Note 3:	*ML8.d.3. does not control iodine pentafluoride (CAS 7783-66-6).*";

(h) in the Technical Notes to entry ML8.h., before paragraph 1 on a new line, insert "*For the purposes of ML8.h.:*";

(i) in the Technical Note to entry ML9.a.2.a.—

(i) for "*'Mountings'*" substitute "*For the purposes of ML9.a.2.a., 'mountings'*";

(ii) for "*purpose of*" substitute "*purposes of*";

(j) in entry ML9.a.2.c. for the Technical Notes, substitute—

(**1**) S.I. 2008/3231; relevant amending instruments are S.I. 2010/2007, 2012/1910, 2014/1069, 2015/940, 2017/85, 697, 2018/165, 939, 2019/137, 989, 1159, 2021/586, 2022/1042, 2023/302.

	"Technical Note:	*For the purposes of ML9.a.2.c.2., 'pre-wet or wash down system' is a seawater spray system capable of simultaneously wetting the exterior superstructure and decks of a vessel.";*

(k) after entry ML9.a.2.d.4., on a new line, insert—

	"Technical Note:	*For the purposes of ML9.a.2., 'CBRN protection' is a self-contained interior space containing features such as over-pressurisation, isolation of ventilation systems, limited ventilation openings with CBRN filters and limited personnel access points incorporating air-locks. ";*

(l) in entry ML17.e.3., for "electro-magnetic pulse (EMP)" substitute "'electromagnetic pulse' ('EMP')";

(m) in the Technical Note to entry ML17.e.3., for "*Electro-magnetic pulse*" substitute "*For the purposes of ML17.e.3., 'EMP'*";

(n) in entry ML18.a.—

    (i) at the beginning, for "Specially" substitute "Equipment specially";

    (ii) omit "production equipment";

(o) for entry ML18.b. substitute—

	"b.	Environmental test facilities, specially designed for the certification, qualification or testing of goods specified in this Schedule, and specially designed equipment therefor, not specified elsewhere in this Schedule";

(p) in entry PL5001.f., for "*article 9*" substitute "*article 42S*".

(3) In Schedule 3 (UK Controlled Dual-Use Goods, Software and Technology)—

(a) in the section headed "Definitions" insert at the appropriate place—

""circuit element" is a single active or passive functional part of an electronic circuit, such as one diode, one transistor, one resistor, one capacitor, etc;";

""digital computer" means equipment which can, in the form of one or more discrete variables, perform all of the following—

<div align="center">a. Accept data;</div>

b. Store data or instructions in fixed or alterable (writable) storage;

c. Process data by means of a stored sequence of instructions which is modifiable; and

d. Provide output of data;

Note: Modifications of a stored sequence of instructions include replacement of fixed storage devices, but not a physical change in wiring or interconnections;";

""discrete component" is a separately packaged "circuit element" with its own external connections;";

""electronic assemblies" means a number of electronic components (i.e., "circuit elements", "discrete components", integrated circuits, etc.) connected together to perform (a) specific function(s), replaceable as an entity and normally capable of being disassembled;";

"Process Design Kit" ("PDK") is a software tool provided by a semiconductor manufacturer to ensure that the required design practices and rules are taken into account in order to successfully produce a specific integrated circuit design in a specific semiconductor process, in accordance with technological and manufacturing constraints (each semiconductor manufacturing process has its particular "PDK");";

(b) after entry PL9012 on a new line insert—

"

Electronics and related equipment, materials, software and technology

PL9013 The export or "transfer by electronic means" of the following goods, "software" or "technology", is prohibited to any destination:

a. Systems, equipment and components, as follows:

1. Complementary Metal Oxide Semiconductor (CMOS) integrated circuits, not controlled in 3A001.a.2. in Annex I to "the dual-use Regulation", designed to operate at an ambient temperature equal to or less (better) than 4.5 K (-268.65°C).

Note: The status of wafers (finished or unfinished), in which the function has been determined, are to be evaluated against the parameters of PL9013.a.1.

Technical note:

For the purposes of PL9013.a.1., CMOS integrated circuits are also referred to as

cryogenic CMOS or cryoCMOS integrated circuits.

2. Equipment designed for dry etching, having any of the following:

    a. Equipment designed or modified for isotropic dry etching, having a largest 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' of greater than or equal to 100:1; or

    b. Equipment designed or modified for anisotropic dry etching, having all of the following:

        1. Radio Frequency (RF) power source(s) with at least one pulsed RF output;

        2. One or more fast gas switching valve(s) with switching time less than 300 ms; and

        3. Electrostatic chuck with 20 or more individually controllable variable temperature elements.

        Note 1: *PL9013.a.2. includes etching by 'radicals', ions, sequential reactions or non-sequential reactions.*

        Note 2: *PL9013.a.2.b. includes*

etching using RF pulse excited plasma, pulsed duty cycle excited plasma, pulsed voltage on electrodes modified plasma, cyclic injection and purging of gases combined with a plasma, plasma atomic layer etching or plasma quasi-atomic layer etching.

Technical Notes:

1.   For the purposes of PL9013.a.2.a., 'silicon germanium-to-silicon (SiGe:Si) etch selectivity' is measured for a Ge concentration of greater than or equal to 30% ($Si_{0.70}Ge_{0.30}$).

2.   For the purposes of PL9013.a.2. Note 1., 'radical' is defined as an atom, molecule or ion that has an unpaired electron in an open electron shell configuration.

3.   Scanning Electron Microscope (SEM) equipment designed for imaging semiconductor devices or integrated circuits, having all of the following:

a.   Stage placement accuracy less (better) than 30 nm,

b.   Stage positioning measurement performed using laser interferometry,

c.   Position calibration within a Field-Of-View (FOV) based on laser interferometer length-scale measurement,

d.   Collection and storage of images having more than 2×10^8 pixels,

e.   FOV overlap of less than 5% in vertical and horizontal directions,

f.   Stitching overlap of FOV less than 50 nm, and

g.   Accelerating voltage more than 21 kV.

Note 1:   *PL9013.a.3. includes SEM equipment designed for chip design recovery.*

Note 2:   *PL9013.a.3. does not control SEM equipment designed to accept a Semiconductor Equipment and Materials International (SEMI) standard wafer carrier, such as a 200 mm or larger Front Opening Unified Pod (FOUP).*

4.   Integrated circuits having an aggregate bidirectional transfer rate of 600 Gbyte/s or more over all inputs and outputs and to or from other integrated circuits, not including volatile memories, and having or being programmable to have any of the following:

a.   One or more digital processor units executing machine instructions having a 'total processing performance' of 6000 or more,

b.	One or more digital 'primitive computational units', excluding those units contributing to the execution of machine instructions specified in PL9013.a.4.a., having a 'total processing performance' of 6000 or more,
c.	One or more analogue 'primitive computational units' having a 'total processing performance' of 6000 or more, or
d.	Any combination of digital processor units and 'primitive computational units' on an integrated circuit whose 'total processing performance' across PL9013.a.4.a., PL9013.a.4.b. and PL9013.a.4.c. add up to 6000 or more.

Note: *Integrated circuits specified in PL9013.a.4. include Graphical Processor Units (GPUs), Tensor Processing Units (TPUs), neural processors, in-memory processors, vision processors, text processors, co-processors/accelerators, adaptive processors, Field Programmable Logic Devices (FPLDs) and Application-Specific Integrated Circuits (ASICs).*

Technical Notes:

For the purposes of PL9013.a.4.,

1. *'Total Processing Performance' ('TPP') is the bit length per operation multiplied by the processing performance measured in Tera Operations Per Second (TOPS) over all processor units on the integrated circuit. For example, the 'TPP' for an integrated circuit having two digital processor units that are each capable of 200 TOPS at 16 bits is 6400 (2*

processors × 200 TOPS × 16 bits = 6400). In PL9013.a.4.c., the 'TPP' of each analogue 'primitive computational unit' is the processing performance expressed in TOPS multiplied by 8.

2. A 'primitive computational unit' is defined as containing zero or more modifiable weights, receiving one or more inputs, and producing one or more outputs. A computational unit is said to perform 2N-1 operations whenever an output is updated based on N inputs, where each modifiable weight contained in the processing element counts as an input. Each input, weight, and output might be an analogue signal level or a scalar digital value represented using one or more bits. Such units include:

Artificial neurons

Multiply accumulate (MAC) units

Floating-Point Units (FPUs)

Analogue multiplier units

Processing units using memristors, spintronics, or magnonics

Processing units using photonics or non-linear optics

Processing units using analogue or multi-level

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non-volatile weights

Multi-value or multi-level units

Spiking units

3.	*Operations relevant to the calculation of TOPS include both scalar operations and the scalar constituents of composite operations such as vector operations, matrix operations, and tensor operations. Scalar operations include integer operations, floating-point operations (often measured by FLOPS), fixed-point operations, bit-manipulation operations and/or bitwise operations.*
4.	*The rate of TOPS is the maximum value theoretically possible when all processing units are operating simultaneously. The rate of TOPS and aggregate bidirectional transfer rate is assumed to be the highest value the manufacturer claims in a manual or brochure for the chip.*
5.	*The bit length of an operation is equal to the highest bit length of any input or output of that operation. Additionally, if the processor unit is designed for operations that achieve different bits × TOPS values, the highest bits × TOPS value should be used.*
6.	*For processing units that provide processing of both sparse and dense matrices, the TOPS values are the values for processing of dense matrices (e.g., without sparsity).*
N.B.:	*For "digital computers" and "electronic assemblies"*

<p style="text-align:right">*containing integrated circuits specified in PL9013.a.4., see PL9014.a.2*</p>

5. Parametric signal amplifiers having all of the following:

  a. Designed for operation at an ambient temperature below 1 K (-272.15ºC),

  b. Designed for operation at any frequency from 2 GHz up to and including 15 GHz, and

  c. A noise figure less (better) than 0.015 dB at any frequency from 2 GHz up to and including 15 GHz at 1 K (-272.15ºC).

  Note: Parametric signal amplifiers include Travelling Wave Parametric Amplifiers (TWPAs).

Technical Note:

For the purposes of PL9013.a.5., parametric signal amplifiers may also be referred to as Quantum-Limited Amplifiers (QLAs).

6. Cryogenic cooling systems and components, as follows:

  a. Systems rated to provide a cooling power greater than or equal to 600 µW at or below a temperature of 0.1 K (-273.05°C) for a period of greater than 48 hours;

  b. Two-stage pulse tube cryocoolers rated to maintain a temperature below 4 K (-269.15°C) and provide a cooling power greater than or equal to 1.5 W at or below a temperature of 4.2 K (-268.95°C).

7. 'Extreme Ultraviolet' ('EUV') masks and 'EUV' reticles, designed for integrated circuits, other than those specified in 3B001.g. in Annex I to "the dual-use Regulation", and having a mask 'substrate blank' specified in 3B001.j. in Annex I to "the dual-use Regulation";

Technical Notes:

For the purposes of PL9013.a.7.,

1.   Masks or reticles with a mounted pellicle are considered masks and reticles. A pellicle is a membrane integrated with a frame, designed to protect a mask or reticle from particle contamination.

2.   'Extreme Ultraviolet' ('EUV') refers to electromagnetic spectrum wavelengths greater than 5 nm and less than 124 nm.

3.   'Substrate blanks' are monolithic compounds with dimensions suitable for the production of optical elements such as mirrors or optical windows.

8.   Cryogenic wafer probing equipment having all of the following:

a.   Designed to test devices at temperatures less than or equal to 4.5 K (-268.65°C); and

b.   Designed to accommodate wafer diameters greater than or equal to 100 mm.

b.   Materials as follows:

1.   Epitaxial materials consisting of a 'substrate' having at least one epitaxially grown layer of any of the following:

a.   Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30; or

b.   Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

2.   Fluorides, hydrides, or chlorides of silicon or germanium, containing any of the following:

a.   Silicon having an isotopic impurity less than 0.08% of

			silicon isotopes other than silicon-28 or silicon-30; or
		b.	Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.
	3.		Silicon, silicon oxides, germanium or germanium oxides, containing any of the following:
		a.	Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30; or
		b.	Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

Note:

PL9013.b.3. includes 'substrates', lumps, ingots, boules and preforms.

Technical Note:

For the purposes of PL9013.b., 'substrate' is a sheet of base material with or without an interconnection pattern and on which or within which "discrete components" or integrated circuits or both can be located.

c.	"Software" as follows:	
	1.	"Software" specially designed for the "development" or "production" of equipment specified in PL9013.a.2., PL9013.a.3., PL9013.a.5., PL9013.a.7. or PL9013.a.8.
	2.	"Software" specially designed for the "use" of equipment specified in PL9013.a.2.
	3.	"Software" designed to extract 'Geometrical Database Standard II' ('GDSII') or equivalent standard layout data and perform layer-to-layer alignment from Scanning Electron Microscope (SEM) images, and generate multi-layer 'GDSII' data or the circuit netlist.

Technical Note:

> *For the purposes of PL9013.c.3., 'Geometrical Database Standard II' ('GDSII') is a database file format for data exchange of integrated circuit or integrated circuit layout artwork.*

d.   "Technology" as follows:

1.   "Technology" according to the General Technology Note in Annex I to "the dual-use Regulation" for the "development" or "production" of equipment or materials specified in PL9013.a.1., PL9013.a.2., PL9013.a.3., PL9013.a.4., PL9013.a.5., PL9013.a.6., PL9013.a.7., PL9013.a.8. or PL9013.b.

Note: PL9013.d.1. does not control "Process Design Kits" ("PDKs").

2.   "Technology" according to the General Technology Note in Annex I to "the dual-use Regulation" for the "development" or "production" of integrated circuits or devices, using 'Gate all-around Field-Effect Transistor' ('GAAFET') structures.

Note 1:   *PL9013.d.2. includes 'process recipes'.*

Technical Note:

For the purposes of PL9013.d.2. Note 1., a 'process recipe' is a set of conditions and parameters for a particular process step.

Note 2:   *PL9013.d.2. does not control tool qualification or maintenance "technology".*

Note 3:   *PL9013.d.2. does not control "Process Design Kits" ("PDKs").*

Technical Note:

For the purposes of PL9013.d.2., 'Gate all-around Field-Effect Transistor' ('GAAFET') means a device having a single or multiple semiconductor conduction channel element(s) with a common gate structure that surrounds and controls current in all of the semiconductor conduction channel elements.

Note: *This definition includes nanosheet or nanowire field-effect and surrounding gate transistors and other*

'GAAFET' semiconductor channel element structures.

Computers and related equipment, materials, software and technology

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PL9014   The export or "transfer by electronic means" of the following goods, "software" or "technology", is prohibited to any destination:

   a.   Systems, equipment and components, as follows:

      1.   Quantum computers and related "electronic assemblies" and components therefor, as follows:

         a.   Quantum computers as follows:

            1.   Quantum computers supporting 34 or more, but fewer than 100, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 10^{-4};

            2.   Quantum computers supporting 100 or more, but fewer than 200, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 10^{-3};

            3.   Quantum computers supporting 200 or more,

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	but fewer than 350, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 2×10^{-3};
4.	Quantum computers supporting 350 or more, but fewer than 500, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 3×10^{-3};
5.	Quantum computers supporting 500 or more, but fewer than 700, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 4×10^{-3};
6.	Quantum computers supporting 700 or more, but fewer than 1,100, 'fully controlled',

'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 5 x 10^{-3}.;

7. Quantum computers supporting 1,100 or more, but fewer than 2,000, 'fully controlled', 'connected' and 'working' 'physical qubits', and having a 'C-NOT error' of less than or equal to 6 x 10^{-3}.;

8. Quantum computers supporting 2,000 or more 'fully controlled', 'connected' and 'working' 'physical qubits';

b. Qubit devices and qubit circuits, containing or supporting arrays of 'physical qubits', and specially designed for items specified in PL9014.a.1.a.;

c. Quantum control components and quantum measurement devices, specially designed for items specified in PL9014.a.1.a.

Note 1: *PL9014.a.1. includes circuit model (or gate-based) and one-way (or measurement-based) quantum computers.*

Note 2:	*PL9014.a.1. does not control adiabatic (or annealing) quantum computers.*
Note 3:	*Items specified in PL9014.a.1. may not necessarily physically contain any qubits. For example, quantum computers based on photonic schemes do not permanently contain a physical item that can be identified as a qubit. Instead, the photonic qubits are generated while the computer is operating and then later discarded.*
Note 4:	*PL9014.a.1.b. includes the following:*

> *semiconductor, superconducting, and photonic qubit chips and chip arrays;*
>
> *surface ion trap arrays;*
>
> *other qubit confinement technologies; and*
>
> *coherent interconnects between such items.*

Note 5:	*PL9014.a.1.c. includes items designed for calibrating, initialising, manipulating or measuring the resident qubits of a quantum computer.*

Technical Notes:

For the purposes of PL9014.a.1.:

1.	*A 'physical qubit' is a two-level quantum system used to represent the elementary unit of quantum logic by means of manipulations and measurements that are not error corrected. 'Physical qubits' are distinguished from*

		logical qubits, in that logical qubits are error-corrected qubits comprised of many 'physical qubits'.
	2.	*'Fully controlled' means the 'physical qubit' can be calibrated, initialised, gated, and read out, as necessary.*
	3.	*'Connected' means that two-qubit gate operations can be performed between any arbitrary pair of the available 'working' 'physical qubits'. This does not necessarily entail all-to-all connectivity.*
	4.	*'Working' means that the 'physical qubit' performs universal quantum computational work according to the system specifications for qubit operational fidelity.*
	5.	*Supporting 34 or more 'fully controlled', 'connected', 'working' 'physical qubits' refers to the capability of a quantum computer to confine, control, measure and process the quantum information embodied in 34 or more 'physical qubits'.*
	6.	*'C-NOT error' is the average physical gate error for the nearest-neighbour two-'physical qubit' Controlled-NOT (C-NOT) gates.*

	2.	Computers, "electronic assemblies" and components containing one or more integrated circuits specified in PL9013.a.4.
	Note:	*Computers include "digital computers", hybrid computers, and analogue computers.*

b.	Materials as follows:
	This entry is not used.

c.	"Software" as follows:
	1.	"Software" specially designed or modified for the "development" or "production"

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of equipment specified in PL9014.a.1.b., PL9014.a.1.c. or PL9014.a.2.

d.   "Technology" as follows:

1.   "Technology" according to the General Technology Note in Annex I to "the dual-use Regulation" for the "development" or "production" of equipment specified in PL9014.a.1.b., PL9014.a.1.c. or PL9014.a.2, or software specified in PL9014.c.1.

2.   "Technology" according to the General Technology Note in Annex I to "the dual-use Regulation" for the "use" of equipment specified in PL9014.a.2.

Materials processing and related equipment, materials, software and technology

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PL9015   The export or "transfer by electronic means" of the following goods, "software" or "technology", is prohibited to any destination:

a.   Systems, equipment and components, as follows:

1.   Additive manufacturing equipment, designed to produce metal or metal alloy components, having all of the following, and specially designed components therefor:

a.   having at least one of the following consolidation sources:

1.   'Lasers';

2.   Electron beam; or

3.   Electric arc;

b.   having a controlled process atmosphere of any of the following:

1.   Inert gas; or

2.   Vacuum (equal to or less than 100 Pa);

c.   having any of the following 'in-process monitoring' equipment in a 'co-axial configuration' or 'paraxial configuration':

1.   Imaging camera with a

peak response in the wavelength range exceeding 380 nm but not exceeding 14,000 nm;

2. Pyrometer designed to measure temperatures greater than 1,273.15 K (1,000°C); or

3. Radiometer or spectrometer with a peak response in the wavelength range exceeding 380 nm but not exceeding 3,000 nm; and

d. A closed loop control system designed to modify the consolidation source parameters, build path, or equipment settings during the build cycle in response to feedback from 'in-process monitoring' equipment specified in PL9015.a.1.c.

Technical Notes

For the purposes of PL9015.a.1.,

1. *'Laser' is an item that produces spatially and temporally coherent light through amplification by stimulated emission of radiation.*

2. *'In-process monitoring', also known as in-situ process monitoring, pertains to the observation and measurement of the additive manufacturing process including electromagnetic or thermal emissions from the melt pool.*

3.   *'Co-axial configuration', also known as on-axis or inline configuration, pertains to one or more sensors that are mounted in an optical path shared by the 'laser' consolidation source.*

4.   *'Paraxial configuration' pertains to one or more sensors that are physically mounted onto or integrated into the 'laser', electron beam or electric arc consolidation source component.*

5.   *For both 'co-axial configuration' and 'paraxial configuration', the field of view of the sensor(s) is fixed to the moving reference frame of the consolidation source and moves in the same scan trajectories of the consolidation source throughout the build process.*

b.   Materials as follows:

This entry is not used.

c.   "Software" as follows:

1.   "Software" specially designed or modified for the "development" or "production" of equipment specified in PL9015.a.1.

d.   "Technology" as follows:

1.   "Technology" according to the General Technology Note in Annex I to "the dual-use Regulation" for the "development" or "production" of equipment specified in PL9015.a.1. or software specified in PL9015.c.1.

2.   "Technology", not specified in Annex I to "the dual-use Regulation", for the "development" or "production" of 'coating systems' having all of the following:

a.   Designed to protect ceramic 'matrix' 'composite' materials specified in 1C007 in Annex I to "the dual-use Regulation" from corrosion; and

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| | b. | Designed to operate at temperatures exceeding 1,373.15 K (1,100#). |

Technical Notes:

For the purposes of PL9015.d.2.:

1.	*'Coating systems' consist of one or more layers (e.g., bond, interlayer, top coat) of material deposited on the substrate.*
2.	*'Matrix' means a substantially continuous phase that fills the space between particles, whiskers or fibres.*
3.	*'Composite' means a 'matrix' and an additional phase or additional phases consisting of particles, whiskers, fibres or any combination thereof, present for a specific purpose or purposes."*.